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EXAMINER	
HO, THOMAS M	

ART UNIT	PAPER NUMBER
2134	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/672,367	MCKEEN ET AL.	
	Examiner	Art Unit	
	Thomas M. Ho	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *29 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are pending.

Response to Arguments

2. The rejection of 2/10/2005 was inadvertently made final. The Examiner had agreed with the attorney Thomas Coester over the telephone that the finality was indeed improper. Accordingly the finality of the rejection of 2/10/2005 has been withdrawn.

Applicant has the following regarding the rejection of 2/10/05:

(Arguments, pages 5&6)

In regards to claims 1, Applicants submit that neither Pai nor the PC guide separately or in combination, teaches or suggests system memory including an isolated output area. Rather, Pai teaches a display buffer driven by a video display card (Fig. 1 and col. 3, lines 61-63), and the PC guide teaches the sharing of a system memory with a video chipset. Combining Pai with the PC guide would at most place the video card memory in the system memory, but would not isolate a portion of the system to include an isolated output area.

However, modifying Pai, to place the display buffer in the system memory would render the display buffer accessible by processes or devices that share access to the system memory.

The Examiner disagrees with Applicant's assertion. Pai teaches a video memory which the Examiner has characterized as isolated. PC Guide teaches that the main system memory is shared with the video subsystem to allow that video subsystem access to the greater memory. It is a mischaracterization of the combination under 35 USC 103 that the video card memory would be placed into the system memory. PC (Second sentence) states that the video card has access to the system memory for its functions. This DOES NOT mean however that this would render the display buffer accessible to processes or devices. Nowhere does Pai teach that access by the video to the system memory thereby allows system memory access to the video memory such as the buffer. In this sense, the examiner has characterized the video memory from the combination as system memory. Furthermore Pai would appear to teach against Applicant's characterization of the combination: (second paragraph, last sentence) "The frame buffer is the most important part of the video memory and it requires the highest performance, so it makes sense to leave it on the video card so special video-specific technologies like VRAM can be used.

This is different from characterizing system memory as video memory which the Applicant appears to be advocating.

Applicant continues to argue (page 6, paragraph 2)

Additionally, Applicant's respectfully contend the Examiner's characterization of a monitor as the isolated output area of the system memory. A monitor is a peripheral device and its memory is peripheral memory. According to common knowledge in the art, peripheral memory is physically separated from system memory and is generally implemented with technology

specifically suited for the function of the peripheral device. Thus, a monitor cannot be part of the system memory.

The Examiner has acknowledged Applicant's reasoning above. Indeed it was for that reason that the original rejection had been withdrawn in the first place. However, PC Guide "AGP Video System Memory Access" is new innovation with certain advantages that explicitly teaches otherwise. A monitor accesses video memory. This is clearly shown in Pai, figure 1. PC guide teaches an embodiment that incorporates the system memory and video memory together in that the video memory now has access to the system memory. (It does not teach the converse embodiment that Applicant advocates) The special technology advocated by PC Guide would indeed allow a monitors memory (frame buffer and video memory) to be system memory.

Applicant argues page 6, last paragraph :

Applicants submit that Pai at least fails to teach or suggest an isolated mode. At most, Pai teaches preventing direct access to the genetic code memory by processors or master devices.

The Examiner contends that preventing such access is precisely how an "isolated mode" is understood in the art, that is, under some conditions access to a particular resource would be restricted.

Applicant's further arguments are unpersuasive and merely allege what the rejections do not disclose without providing evidence nor disclosure from the specification.

Finally the Examiner argues that the combination made by 35 USC 103 must have some presumption that one of ordinary skill in the art would take the appropriate measures to combine certain inventions provided that it was advantageous and within his or her skill to do so. Applicant previously argued:

However, modifying Pai, to place the display buffer in the system memory would render the display buffer accessible by processes or devices that share access to the system memory.

Such an argument would be similar to arguing that it would not be obvious to combining a computer with a power switch, because no wire is present to connect the switch to the computer. The Examiner contends that at least some presumption is necessary that one of ordinary skill in the art would take the necessary steps to secure a combination provided that it was within his or her skill to do so.

It is an improper characterization of the rejection to deliberately interpret a combination into inoperability.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pai et al. and Pcguide.

In reference to claim 1:

Pai et al. discloses a platform comprising:

- A processor executing in one of a normal execution mode and an isolated execution mode, where the processor executes the software for displaying critical data, but is isolated from the actual data both physically and logically. (Column 3, lines 10-40)
- A memory including an isolated area, an isolated output area, and a non-isolated area, where the memory contains the genetic code, is isolated from access by the processor, and the output area is the monitor, as is isolated from both processor and software access. (Column 2, lines 57-60)
- An output device, where the output device may either be the video card or the monitor display. (Column 3, line 62- Column 4, line 1)

Pai et al. however does not disclose that the video card memory is system memory, but rather discloses the functions of the isolated execution take place in the video memory.

The PC guide("AGP Video System Memory Access"), however discloses a technique called AGP video system memory access, in which the video function are performed on system memory. The functions normally performed on the video card, are performed on the system memory, providing the advantage of allowing larger amounts of memory for 3D and other processing, without requiring that large quantities of special video memory be put on the video card.

It would have been obvious to one of ordinary skill in the art at the time of invention to use this "AGP video system memory access" in which the video functions performed by the video memory of Pai was performed in regular system memory in order to provide the advantage advantage of allowing larger amounts of memory for 3D and other processing, without requiring that large quantities of special video memory be put on the video card.

In reference to claim 2:

Pai et al. (Column 3, line 62- Column 4, line 1) discloses the platform of claim 1 wherein the output device is a graphics card, where the data is first given to the video card, which outputs the data to the monitor.

In reference to claim 3:

The platform of claim 2 further comprising:

Pai et al. Figure 3 discloses a memory control hub (MCH) coupled between the system memory, and the processor and the graphics card, the memory control hub to permit the graphics card to access the isolated output area only when the graphics card is in isolated access mode, where the memory control hub is the Input synchronization mode registers and the switches, which controls and regulates the access to the isolated output area, the link between the memory and the control hub, and permits the graphics card to access that area only when the graphics card is in isolated mode. (Column 5, lines 20-50)

In reference to claim 4:

Pai et al. discloses the platform of claim 3 wherein the graphics card comprises:

(Column 4, lines 44-48) & (Column 5, lines 45-50) A direct memory access (DMA) controller and wherein local storage of the data from the isolated output area is not permitted, where the access of that stored data containing the genetic code is not permitted, and the DMA controller is understood to be there in order to be able to access the memory(display buffer) and its video card memory.

In reference to claim 5:

Pai et al. (Column 5, lines 5-50) discloses the platform of claim 3 wherein only the graphics card is permitted to read the isolated output area, where the graphics card reads the isolated output area by having the output area send the genetic code to the display buffer.

In reference to claim 6:

The platform of claim 1 further comprising:

Pai et al. (Column 4, lines 49-57) An operating system (O/S) nub having a driver to write display data into the isolated output area when the processor is executing in isolated execution mode, where the driver writes the display data into the isolated output area, the monitor.

In reference to claim 7:

Pai et al. (Figure 2) The platform of claim 3 further comprising:

A link between the graphics card and the MCH having an isolated transaction type, where the MCH is the Input mode synchronization registers and the hardware switches for controlling the isolated transactions, and the transactions it performs are isolated transactions. (Column 4, line 49 – Column 50, line 50)

In reference to claim 8:

(Column 4, lines 49-57) The platform of claim3 wherein the MCH only permits the O/S nub to write the isolated output area, where the OS nub which writes to the isolated output area is the software controlling the writing, or the video driver.

In reference to claim 9:

Pai et al. (Figure 3) The platform of claim 7 wherein the link is a secure accelerated graphics port bus, where the bus is the data line, inherently present connecting the video card with the MCH, where the line is secure since neither the processor nor the software can access the data, and

where the bus is an accelerated graphics port since all video cards are graphics acceleration devices.

In reference to claim 10:

Pai et al. (Column 5, lines 40-50) discloses the platform of claim 2 wherein the graphics card comprises:

An isolated bit, where the isolated bit plane is the video buffer under the isolated execution mode where the video buffer inherently constitutes a plane of bits.

A non-isolated bit plane, where the non-isolated bit plane is the video buffer under the normal execution mode.

In reference to claim 11:

Pai et al. (Column 5, lines 40-50) discloses the platform of claim 10 wherein the graphics card denies all external access to the isolated bit plane, where all access to isolated bit plane is prevented.

In reference to claim 12:

Pai et al. discloses a method comprising:

- Establishing an isolated execution environment having an isolated execution mode, where the isolated execution mode is the mode of execution wherein the genetic code is

contained on the memory and cannot be accessed by external processes. (Column 3, lines 10-40)

- Preventing access to output data by any requester not operating in an isolated mode, where the requestors not operating in the isolated mode are the external processors. (Column 2, lines 57-60)

Claim 13 is rejected for the same reasons as claim 1.

In reference to claim 14:

Pai et al.(Figure 1) (Column 4, line 49 – Column 5, line 50) discloses the method of claim 13 further comprising:

(Column 5, lines 2-35) Issuing an isolated direct memory access (DMA) request for display data in the isolated output area from a graphics card, where the isolated memory is isolated in that it cannot be read by any other devices and the display data is located in the display buffer of the video card, and the isolated DMA request for display data from the graphics card is read until it is fully output to the monitor.

Refreshing the display based on the display data, where the display buffer is the memory that is used to refresh monitor displays.

In reference to claim 15:

Pai et al. (Column 4, line 49 – Column 5, line 50) discloses the method of claim 13 wherein preventing comprises:

- Identifying if an isolated attribute is present in a request for access to the isolated output area, where the isolated attribute is any one of the starting mechanisms that initiates the GDP, the value of the synchronization mode logic, or the value of the enable signal of the data switch device.
- Denying the request if no isolated attribute is present(Column 5, lines 19-31), where the data is never transferred if the display mode synchronization logic or the EN signal isn't set.

In reference to claim 16:

Pai et al. (Column 5, lines 40-50) discloses the method of claim 13 further comprising:

- Loading data from the isolated output area into a bit plane on a graphics card, where the bit plane is the display buffer, and the isolated output area can be the genetic code memory. (Figure 1)
- Denying all external access to the bit plane, where the access to the graphics buffer is denied to other components.

In reference to claim 17:

Pai et al. (Figure 1) discloses the method of claim 16 further comprising:

- Defining a first window for display of an image corresponding to the bit plane, where the image displayed is displayed in a first window corresponding to the bit plane or the video buffer.

- Occluding all windows but the first window, where all other windows in the display of figure 1 are occluded except the first window.

In reference to claim 18:

Pai et al. (Figure 1) discloses the method of claim 13 further comprising:

- Retrieving data from the isolated output area, where the data is retrieved from the genetic code memory.
- Displaying an image corresponding to the data, where the image is displayed on a monitor.
- Pai et al. fails to explicitly disclose
- Occluding the image prior to a platform transitioning out of isolated execution mode.

The Examiner takes official notice that such occlusion of a user exiting an isolated execution mode are well known in the art. ATM machines for example, occlude or close any windows containing data pertinent to the user's bank account prior to it fully transitioning out (before you are given a receipt of your balance)

It would have been obvious to one of ordinary skill in the art the occlude the image prior to transitioning out of isolated execution mode, in order to preserve the security of the information being displayed.

In reference to claim 19:

Pai et al. discloses a platform comprising:

- A processor executing in one of a normal execution mode and an isolated execution mode; (Column 3, lines 10-40) & (Column 2, lines 57-60)
- A direct memory access (DMA) controller to issue requests for access to an isolated output area; (Column 4, lines 44-48) & (Column 5, lines 45-50)
- A first interface coupled to the DMA controller to forward requests to a memory control hub (MCH); (Column 5, lines 20-50)

Pai et al. fails to disclose a second interface coupled to the DMA controller to supply output data to an output device.

The examiner takes official notice that second interfaces coupled to a DMA controller to supply output data to additional output devices was well known at the time of invention. Examples include computers that have both a video card, and a sound card, or computers with more than one video card.

It would have been obvious to one of ordinary skill in the art at the time of invention to disclose a second interface coupled to the DMA controller to supply output data to an output device, in order to allow more than one output.

In reference to claim 20:

Pai et al. discloses all of claim 20 except an interface using an AGP slot.

The examiner takes official notice that AGP interfaces were well known to those of ordinary skill in the art at the time of invention. In fact, AGP slots were and still are the prevalent graphics interface port in computers.

It would have been obvious to one of ordinary skill in the art at the time of invention to use an interface that was a secure AGP slot for the video card to be attached to, because they are the most widely used video card interface today, and would consequently be compatible with the video cards produced by other vendors in industry.

In reference to claim 21:

Pai et al. (Column 4, line 49 – Column 5, line 50) discloses the apparatus of claim 19 wherein the DMA controller attaches an isolated attribute to any isolated output area access request, where the memory request is made with the initialization of the GDP, the activation of switches, and is dependent on the current enable value of display mode synchronization logic signal.

In reference to claim 22:

Pai et al. fails to disclose the apparatus of claim 19 wherein the second interface is an audio interface.

The examiner takes official notice that audio interfaces were well known to those of ordinary skill in the art at the time of invention.

It would have been obvious to one of ordinary skill in the art at to time of invention to have an audio interface coupled to the DMA controller to supply output data to an output device, to allow audio data to be output, as opposed to simply video.

Conclusion

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of the final action and the advisory action is not mailed under after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension pursuant to 37 CFR 1.136(A) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication from the examiner should be directed to Thomas M Ho whose telephone number is (571)272-3835. The examiner can normally be reached on M-F from 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory A. Morse can be reached on (571)272-3838.

The Examiner may also be reached through email through Thomas.Ho6@uspto.gov

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

General Information/Receptionist	Telephone: 571-272-2100	Fax: 703-872-9306
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TMH

July 10th, 2005